

REMARKS

This paper is responsive to the Non-Final Office Action dated September 8, 2005. Claims 1-151 were examined. Claims 1-9, 11-14, 26-44, 46-49, 61-83, 85-88, 100-120, 122-125, and 137-151 were rejected, and claims 10, 15-25, 45, 50-60, 84, 89-99, 121, and 126-136 were objected to. Applicant thanks the Examiner for a thoughtful examination of the claims.

Claim Rejections - 35 U.S.C. § 112

Claims 11-13, 35, 46-48, 74, 85-87, and 122-124 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 11, 46, 85, and 122, the Examiner has stated that the phrase "... such that both **programmed** and unprogrammed memory cells in the unselected NAND string..." is considered indefinite because there should not be any cell in the unselected string that can be programmed. Applicant agrees that there should not be any cell in the unselected string that is actually programmed, for such would be considered a "disturb" of a memory cell in a non-selected NAND string during programming of memory cell in another NAND string. Much of the description of the instant invention is directed to preventing such disturbances. The reference to a "programmed memory cell in the unselected NAND string" refers to a cell that is currently in a programmed state, having been programmed in a previous operation, even though such cell is not currently selected. Similarly, the reference to an "unprogrammed memory cell in the unselected NAND string" refers to a cell that is currently in an unprogrammed (or erased) state, having been erased in a previous operation or never having been programmed at all, even though such cell is not currently selected.

Regarding claims 35 and 74, the Examiner has stated that "the 'series selection device' is a string selection switch transistor, which is understood not as a memory cell transistor, and consequently cannot be programmed. It can only be turned on or off. Therefore, it is considered unclear how the series selection devices can be programmed to a threshold voltage." Applicant respectfully notes that certain embodiments of the instant invention include one or more series selection devices which are formed substantially identical to the memory cell devices. As such,

these selection devices are fundamentally programmable just like the memory cell devices. The instant application includes description of techniques for ensuring that the threshold voltage of such selection devices is either adjusted to, and/or maintained at, an appropriate voltage. For example, see page 10 at paragraph 1043, and page 20 at paragraph 1066. Applicant has amended claims 35 and 74 to include the limitation that “the memory cell devices and one or more series selection devices forming a given NAND string are structurally substantially identical” to provide greater clarity to the intended limitation.

Applicant respectfully submits that this rejection is overcome, and requests it be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 1-9, 14, 27, 36-44, 49, 75-83, 101, 110, and 112-120 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kanda et al. (U.S. Patent No. 6,522,583 B2). Applicant traverses this rejection in part.

Regarding independent claim 1, Applicant submits that Kanda does not disclose memory cells having a charge storage dielectric. Rather, the disclosed memory cells comprise a floating gate charge storage layer. Likewise, Shimizu et al. does not disclose any such charge storage dielectric layers.

Moreover, claim 1 has also been amended to include the limitation of memory cells comprising thin film switch devices, and further reciting thin film channel regions. Kanda does not disclose such thin film devices or channel regions.

Claim 75 is an analogous apparatus claim, and has likewise been amended, and is likewise believed to be allowable for the same reasons as claim 1.

Regarding claims 3, 38, 77, and 114, Applicant respectfully submits that Kanda does not inherently disclose decoupling adjacent device channel regions. Although Kanda discloses decoupling the half-selected memory cell from a bias source, such as by turning off the block select device, Kanda nowhere describes any functionality which could be construed as

decoupling the half-selected memory cell from adjacent device channel regions after establishing the half-selected memory cell channel region to the first voltage.

Regarding claim 9, 44, 83, and 120, Kanda does not teach the recited limitations. Step (d) must occur before the “capacitively coupling” step (see claim 1), and the cited description and figure do not accomplish such timing, as the passing word line is brought to ground at the end of the boost time, when the selected word line is also brought to ground.

Regarding independent claim 36, Applicant submits that Kanda does not disclose memory cells comprising thin film modifiable conductance switch devices. Moreover, claim 36 has also been amended to recite thin film channel regions. Applicant respectfully submits that Kanda does not describe any such thin film devices or channel regions.

Claim 112 is an analogous apparatus claim, and has likewise been amended, and is likewise believed to be allowable for the same reasons as claim 36.

Regarding claims 11, 46, 85, and 122, Kanda does not disclose a second passing voltage which turns OFF both programmed and unprogrammed memory cells in an unselected NAND string, and such that voltage stress across unselected memory cells in a selected NAND string *is reduced*. To the contrary, Kanda’s second passing voltage is even higher than the Vread voltage, which is described, in certain embodiments, as around 8 volts. By driving the second passing voltage even higher relative to the bit line programming voltage (i.e., ground or VSS), the voltage stress across such unselected memory cells in a selected NAND string is greater, not reduced.

Regarding claim 13, 48, 87, and 124, Kanda does not disclose driving the unselected word lines from the first passing voltage, to ground, and then to the second passing voltage.

Regarding claim 110, Applicant respectfully submits that the Examiner has misunderstood the intended limitations of the claim, for the Examiner has stated that, in Fig. 2, “the strings are shown to be substantially identical.” The claim is intended to recite that the memory cells and the select devices within a given NAND string are substantially identical. In other words, that a select device is substantially identical to a memory cell device. Applicant has amended the claim to now recite “wherein the memory cell devices and one or more series

selection devices forming a given ~~each~~ NAND string are structurally substantially identical.”
Claim 150 has likewise been amended for clarity.

Claim Rejections - 35 U.S.C. § 103

Claims 26, 61, and 100 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanda et al. in view of Choi et al. (U.S. Patent 6,469,933 B2). Applicant respectfully traverses this rejection.

Regarding claim 26 and 61, the cited portion of Choi, et al. describes stepping up the program voltage V_{pgm} to a desired voltage of each program cycle. Although Choi, et al describes multiple programming pulses, there is no description of establishing a bias voltage of a half-selected memory cell channel region before a programming pulse, and likewise no description of re-establishing any such bias voltage before each such programming pulse.

Regarding claim 100, the disclosed apparatus cannot be considered inherent given that the method is not in fact disclosed by Choi et al.

Applicant respectfully requests this rejection be withdrawn.

Claims 28-34, 62-68, 72, 73, 102-108, and 137-143 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanda et al. in view of Shimizu et al. (U.S. Patent 6,115,287). Applicant respectfully traverses this rejection in part.

Regarding claims 29, 66, 67, 103, 141, and 142, Shimizu et al. does not disclose a charge storage dielectric. Rather, a conductive charge storage layer used to fabricate a floating gate is described. For example, Shimizu et al. describes each of the memory cell transistors in Fig. 3C as having a gate insulation film (tunnel oxide film) 14, a floating gate electrode (charge storage layer) 15, an insulation film (e.g., an ONO film) 16, a control gate electrode 17, and an n-type diffusion layer 18 (column 7, lines 31-35). Although an ONO film is described, it is not described as being a charge storage dielectric. Applicant respectfully requests this rejection be withdrawn as to these claims.

Claims 69, 109, 144, and 149 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Forbes (U.S. Patent 6,853,587 B2). In the light of the

believed allowability of the claims from which these rejected claims depend, these claims are believed allowable at least for their dependence from an allowable claim, and thus remain without amendment. Applicant respectfully requests this rejection be withdrawn.

Claims 70, 71, 145, and 146 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Nazarian (U.S. Patent Publication 2005/0111260 A1). In the light of the believed allowability of the claims from which these rejected claims depend, these claims are believed allowable at least for their dependence from an allowable claim, and thus remain without amendment. Applicant respectfully requests this rejection be withdrawn.

Claims 111 and 151 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. In the light of the believed allowability of the claims from which these rejected claims depend, these claims are believed allowable at least for their dependence from an allowable claim, and thus remain without amendment. Applicant respectfully requests this rejection be withdrawn.

Other Amendments to the Claims

Claim 108 was amended to add the word wherein in line 1.

Allowable Subject Matter

Claims 10, 15-25, 45, 50-60, 84, 89-99, 121, and 126-136 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

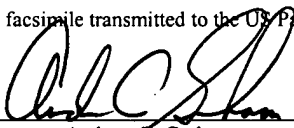
Claims 15, 50, 89, and 126 have been re-written in independent form. Thus, claims 15-25, 50-60, 89-99, and 126-136 are believed to now be fully allowable irrespective of other claims. Claims 15, 50, 89, and 126 also were amended in the last two lines thereof to correct a reference to the unselected NAND string to instead read the selected NAND string.

Claims 10, 45, 84, and 121 remain without amendment.

Summary

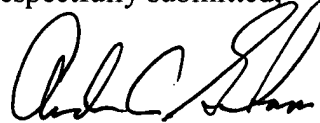
Claims 1-151 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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Respectfully submitted,



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